Delay—Matched Asic Conversion Of A Programmable Logic Device Satwant Singh & Cyrus Tsui M-15198 US

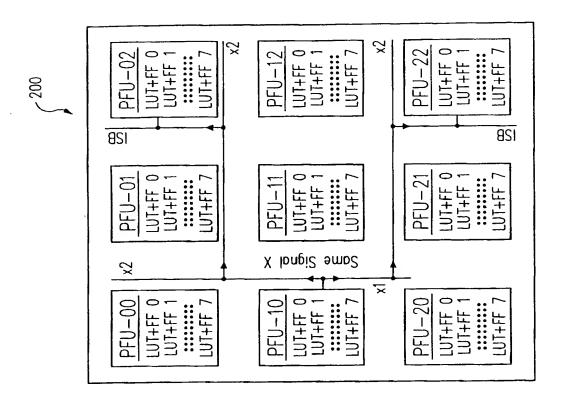
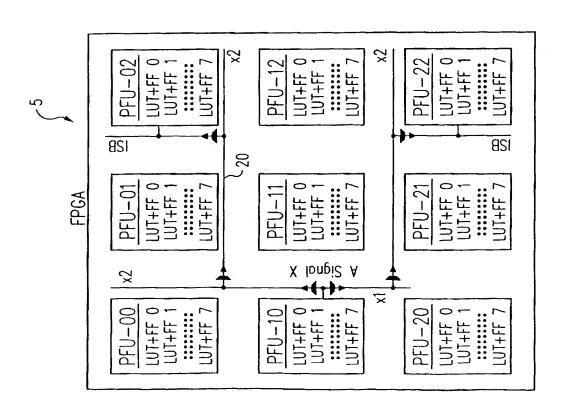


FIG. 2



Delay—Matched Asic Conversion Of A Programmable Logic Device Satwant Singh & Cyrus Tsui M-15198 US 2/5

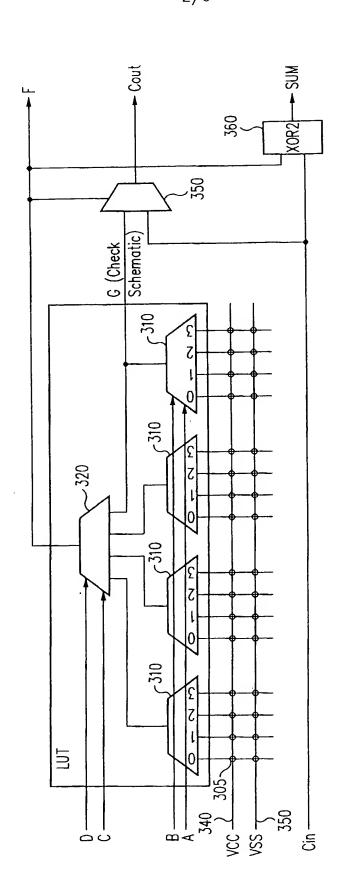
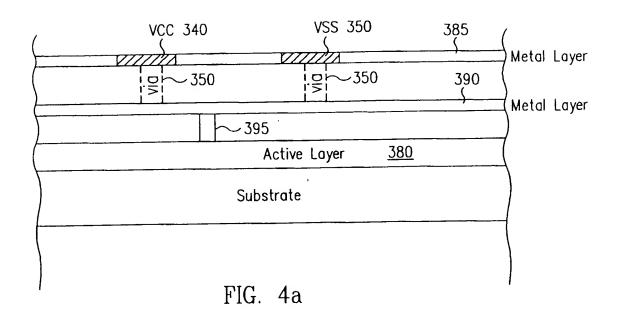
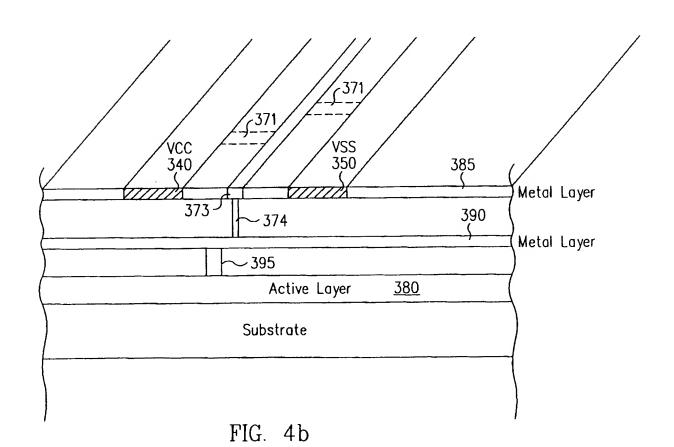


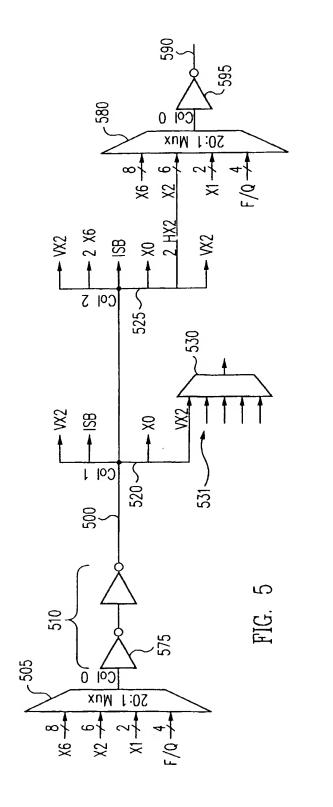
FIG. 3

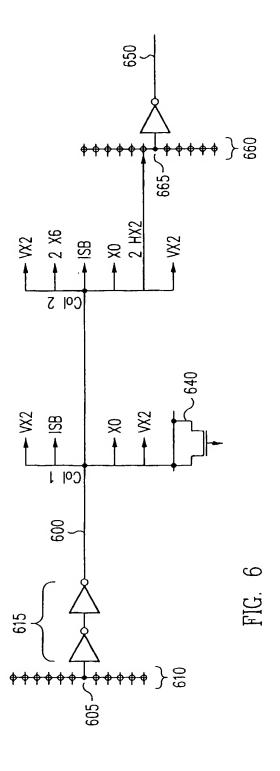
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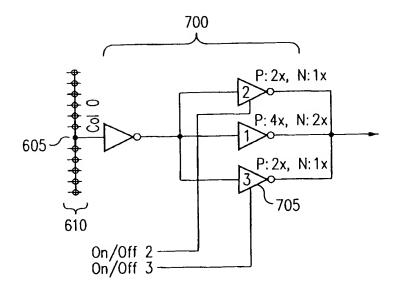


FIG. 7